SDC Performance and Clock Tree Analysis for L476/ChibiOS (16.1)

CPU/DMA (HCLK) speed (MHz)	0.5	1	1	2.5	5	5	5
SDMMC clk speed (MHz)	0.3	0.7	0.8	1.6	2.4	3.2	4.8
eMMC – 4G Micron (v4.51, 153-BGA)							
Single Block Write (kBps)	worked	105	No Go	150	165	171	No Go
Multi-block (128) Write (kBps)	but	177		292	538	623	
Single Block Read (kBps)	timer	335		557	1011	1300	
Multi-block (128) Read (kBps)	issue	351		607	1139	1514	
uSD – 8G Lexar (HC, speed class 10)							
Single Block Write (kBps)	worked	98	No Go	108	154	160	No Go
Multi-block (128) Write (kBps)	but	162		263	464	526	
Single Block Read (kBps)	timer	315		571	1046	1356	
Multi-block (128) Read (kBps)	issue	326		605	1133	1504	

Notes and Issues identified:

1) STM32_SDC_SDMMC_WRITE_TIMEOUT (mcuconf.h) should be 500 (mS) or higher
2) STM32_SDC_SDMMC_READ_TIMEOUT (mcuconf.h) must be 100 (mS) or higher for eMMC ext_csd read
3) Observed write variability of up to .5sec per block. Generally 1 or less blocks experience this, but sometime n
4) SDMMC_CK speed must be 70% slower than AHB speed, i.e. HCLK must be 40% greater than SDMMC_CK
5) RM states that APB2 must also be > 3*BitWidth/32 * SDMMC_CK, BUT believe this is incorrect since: HCLK
6) Code compile issue (IAR) in sdc.c l.322. Need to change const N to a #define. l.120 should clear sdcp->error
7) sdcErase() function not working for either eMMC or uSD (HC SD cardtype). There seem to be several issues

uSD – 8G Lexar current (ave r/w, mA)		23		29	33	34	35
SDMMC_CLKDIV_HS values (w 48MHz SDMMCCLK)	130	60	50	30	20	15	10

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date: Jun 17 2016
file: sdcAnalysis2

10	10	40	40	80	80	80	80
4.8	8	4.8	24	4.8	12	16	24
195	No Go	203		209	228	228	240
850		905		949	1325	1418	1602
1832		1546		1539	2607	2930	4950
2266		2234		2234	5537	6950	10680
189	196	204	222	204	222	222	232
685	797	753	1082	765	998	1050	1109
1939	2951	1947	6081	1947	4005	4804	6146
2241	3668	2241	10099	2241	5382	7022	10095

nore per 12800 block write cycle (on both eMMC and uSD)
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=40, SDMMC_CK=24 with APB2=20 causes underruns
· as sometimes set for eMMC (which think is OK)
, maybe not latest code in 16.1/SDMMCv1??

39	39	47	48	55	55	56	58
10	6	10	2	10	4	3	2